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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
SC13064TH

Certificate of Transmission under 37 CFR 1.8	Application Number	Filed
I hereby certify that this correspondence is being _____ facsimile transmitted or ___X___ e-filed to the United States Patent and Trademark Office - Mail Stop AF. on _____July 27, 2007_____ Signature_____/Dora Hudgins/_____ Typed or printed name: Dora Hudgins	10/728,398	12-05-2003
	First Named Inventor	
	MOYER, WILLIAM C.	
	Art Unit	Examiner
	2113	Elmira Mehrmanesh

Applicant request review of the final rejection in the above identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record.
Registration number: 47,093

☐ attorney or agent acting under 37 CFR 1.34
Registration number if acting under 37 CFR 1.34_____

/Ranjeev Singh/
Signature

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Telephone number

07/27/2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☒ *Total of _____1_____ forms are submitted

REMARKS

STATUS

In a Final Office Action mailed on May 3, 2007, the Examiner maintained rejection of claims 11-24 and 26-34 under 35 U.S.C. § 103(a) based on a combination of Edwards (U.S. Pat. No. 6,484,683) and Steinberg et al. (U.S. Pat. No. 6,966,015) and maintained rejection of claim 25 under 35 U.S.C. § 103(a) based on a combination of Edwards and Steinberg and further in view of Rohfleisch et al. (U.S. Pat. No. 7,058,855);

Pursuant to the guidelines provided by the U.S. PTO in the Official Gazette on July 12, 2005, under the heading "New Pre-Appeal Brief Conference Pilot Program," Applicants are highlighting the clear error related to the rejection of claims 11-34, and is not focusing on other errors.

CLEAR ERROR IN THE REJECTION OF CLAIMS 11-24 AND 26-34 UNDER 35 U.S.C. § 103(a)

Applicants respectfully submit that there is "clear error" in the Examiner's rejection of claims 11-24 and 26-34 because the Examiner has failed to establish a prima facie case of obviousness.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. M.P.E.P. § 2143. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness for at least two reasons. First, the two references, even if combined, which they cannot be, fail to teach or suggest a plurality of functional circuit modules, each functional circuit module being clocked by a clock

that represents a different time domain and having timestamping circuitry, the timestamping circuitry providing a message that indicates a point in time when a predetermined event occurs. The Examiner acknowledges that Edwards does not teach this limitation, and instead contends that Steinberg teaches this limitation. Applicants respectfully disagree with the Examiner's rationale and conclusion for at least the following reasons.

Second, the Examiner has failed to provide evidence of a suggestion or motivation to combine the two references in the manner proposed by the Examiner.

Applicants respectfully submit that the Examiner erroneously equates "time slices" or "multiple discrete time periods," with time domains. Applicants agree with the Examiner that Steinberg teaches monitoring network devices over multiple discrete time periods or time slices, which are used interchangeably in the cited document. (Final Office Action, page 12). **Multiple discrete time periods, however, are not the same as different time domains**.

Time domains, as claimed and as described by Applicants relate to, for example, a clock domain (See, e.g., Specification, page 5, ll. 15-16). Thus, as claimed, claims 11 and 25 require that each of the functional circuit modules has to be clocked by a clock that represents a different time domain. The Examiner relies on col. 6, ll. 53-55 of Steinberg to conclude that Steinberg teaches different time domains. That description, however, relates to monitoring a network device over different discrete time periods or time slices. The time slices taught in Steinberg are generated using a single clock. As explained in Steinberg, status monitors 14 collect data from each managed network element on a fairly continuous basis, e.g., every second or every few seconds. (col. 4, l. 66 – col. 5, l. 3). This data is filtered and is used by correlation engine 22 to perform an edge correlation routine 26 on the filtered data. (col. 5, ll. 19-52). The edge correlation routine compares the transitions of indicators (data related to the condition of a device being monitored) over multiple discrete time periods in step 44. (col. 6, ll. 53-55). In particular, a window of time is divided into a number of discrete time slices and a correlation factor for each time slice is generated. (col. 7, ll. 17-23). The correlation factors for

the various time slices are then combined over the entire window of time ((Fig. 2 shows the window of time with six time slices) to generate a mean correlation factor, for example. (col. 7, ll. 23-28). Thus, Steinberg teaches monitoring and analyzing device conditions over multiple time slices, but does not teach or suggest a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain.

It appears that the Examiner further relies on column 8 and lines 6-9 of Steinberg to conclude that Steinberg teaches or suggests a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain. (Final Office Action, page 13). That description, however, relates to adjusting the timing of a time slice being used. (col. 7, ll. 61-63). In particular, Steinberg notes that the edge correlation technique relies upon the concept of edges transitioning in the same time slice; however, the edges may not transition in the same time slice because of different response times from different monitored devices, for example. (col. 7, ll. 58-62). Steinberg seems to suggest two ways of addressing this problem: (1) increase the size of time slice method, or (2) the "last event time" method. (col. 7, l. 64 – col. 8, l. 65). It is the "last event time" method, which the Examiner relies on to conclude that Steinberg et al. teaches or suggests a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain. That method, however, does not relate to different time domains. The "last event time" method includes: (1) examine, for each time slice, all of the indicators that have changed in that time slice; (2) of those that have changed, look at the one that has changed most recently and look at the last changed time for all of the other indicators; and (3) if any of the other indicators has changed in the same direction in the past 5 seconds from the timestamp of the most recently changed indicator, then consider that indicator to be correlated for the sake of calculating the edge factor. (col. 8, ll. 1-8). Thus, Steinberg teaches edge correlation adjustment mechanisms, but does not teach or suggest a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain, as claimed.

In addition, Applicants respectfully submit that the Examiner relies on the benefit of improper hindsight to combine the two references in the manner proposed by the Examiner. The two references are attempting to solve two unrelated problems. As explained above, unlike Edwards, Steinberg is concerned with reducing false alarms generated by network fault management systems by using an edge correlation routine. The Examiner points to column 18, lines 28-31 to state that Edwards discloses multiple clock cycles. (Final Office Action, page 11, Response to Arguments). This cited section, however, merely notes that at the next microprocessor cycle, after a first watchpoint has been triggered, the state of a latch can be provided an precondition to another watchpoint. (col. 18, ll. 28-31). According to Edwards, in this manner watchpoints can be chained, such that the triggering of one watchpoint can be used to control the triggering of other watchpoints. (col. 18, ll. 31-34). Applicants respectfully submit that this teaching in Edwards would provide no motivation to a person of ordinary skill in the art to combine Edwards with Steinberg.

The Examiner further concludes that "Steinberg's fault monitoring system is a modification of Edwards debugging system by applying continuous monitoring over a plurality of time slices." (Final Office Action, page 12, last line of the first paragraph). Steinberg's network fault management system is an improvement over prior network fault management software tools, such as Netcool/Visionary, which are identified in Steinberg. Apparently, these network fault management software tools like Steinberg's invention are focused on predicting and preventing network faults before they occur. (Steinberg, col. 1, ll. 62-65). These tools, however, have a tendency to generate false alarms. (col. 2, ll. 7-8). To address this problem, Steinberg proposes network fault monitoring over more than one time slice, as explained above. In sum, Steinberg's proposed software system is a modification of conventional network fault management software tools, such as Netcool/Visionary and is not a modification of the Edwards hardware debugging system, as alleged by the Examiner. Thus, contrary to the Examiner's conclusion, a person of ordinary skill in the art will not be motivated to modify Steinberg for use as a time ordering system including a plurality

of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain and having timestamping circuitry, the timestamping circuitry providing a message that indicates a point in time when a predetermined event occurs.

For all of the reasons above, Applicants respectfully request the panel to withdraw the rejection of claims 11-34 based on the cited references.